An Enhanced Flying Capacitor Multilevel Inverter fed Induction Motor Drive

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***Abstract*- This paper focused on the development of capacitor voltage balancing methods in a flying capacitor multilevel inverter (FCMLI) fed induction motor drive. For improving the performance of flying capacitor multilevel inverter, a switching pattern selection scheme is implemented. The proposed method has been designed a nine -level flying capacitor multilevel inverter by using sinusoidal pulse width modulation technique. The selected pattern has been exposed to give superior performance in load voltage, total harmonics distortion and capacitor voltage fluctuation. The performance of proposed strategies is confirmed through simulation investigations.**

***Index Terms* - Total Harmonic Distortion, Flying Capacitor Multilevel Inverter (FCMLI), AC Drive, Sinusoidal pulse width modulation (SPWM).**

I. INTRODUCTION

In recent year, multilevel power inverters are popular due to their high-power, high voltage capacity, low switching losses and low cost. The various different topologies of inverters are neutral point clamped inverters, flying capacitor inverters and cascaded multi level with separated dc source inverter [1]-[2]. Midway the Flying Capacitor Multi-level Inverter (FCMI) does not require isolated dc sides and additional clamping diodes. However, these properties may be quite limited by the voltage unbalancing of flying capacitors which the most serious problem.

[1]Hence the FCMLI has to ensure the voltage balancing of flying capacitors under all the operating conditions. The FCMLI offers a great advantage with respect to the availability of voltage redundancies. They are defined as different combinations of capacitors allowing the charging or discharging of the individual flying capacitors in order to produce the same phase leg voltage. This advantage provides the special opportunity for controlling the individual voltage on flying capacitors [3]-[4]. Many studies have publicized that under certain conditions, a simple open loop control guarantees natural balancing of the flying capacitor.A filter circuit of the *RLC* type tuned at the switching frequency, connected in parallel with the load may be used to achieve the natural balancing under all conditions. However, the extra filter increases the cost of the overall system. Another popular method of capacitor voltage balancing is to vary duty cycles of the switches to charge or discharge the corresponding capacitors. There are many ways such as carrier rotation strategy [5]-[7], modulating signal modification strategy [8], etc. In the control scheme discussed in [9]-[10], balancing is achieved by preferential charging or discharging of the capacitors. This paper highlights sinusoidal PWM based flying capacitor voltage-balancing schemes fed induction motor is discussed. This scheme does not require any modification in the carrier or modulating signal. It has advantage or superiority over other previous works. The modeling of in this paper highlights significance of a nine level FCMLI.

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II.FLYING CAPACITOR MULTILEVEL INVERTER (FCMLI)

The FCMLI requires a large number of capacitors to clamp the device voltage to one capacitor voltage level, provided all the capacitors are equal values. The size of the voltage increases between two consecutive legs of the clamping capacitors. Hence the size of voltage steps in the output waveform.

A. Basic Configuration of FCMLI

A block diagram of nine-level FCMLI is shown in fig 1.It consists of input dc source, switching devices, load and control circuit.

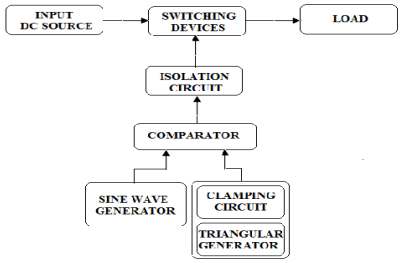

Figure 1. Block diagram for FCMLI.

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The control circuits control the switching devices by using a sinusoidal pulse width modulation (SPWM) strategy.

The voltage of main dc-link capacitor is $V_{dc.}$ The voltage of the capacitor clamping of the innermost two devices are

$$\frac{V_{dc}}{n-1} \quad (1)$$

The voltage of the next innermost capacitor will be

$$\frac{V_{dc}}{n-1}+\frac{V_{dc}}{n-1}=\frac{2V_{dc}}{n-1} \quad (2)$$

Each next clamping capacitor will have the voltage increment of $\frac{V_{dc}}{n-1}$ from its immediate inner one. The voltage levels and the arrangements of the flying capacitor in the FCMLI structure assure the voltage stress across each main device is same. It is equal to $\frac{V_{dc}}{n-1}$ for an n- level inverter.

Three phase of a nine-level inverter fed induction motor as shown in fig 2. A single leg of a nine -level inverter shown in fig 3 and likewise others two are coupled to the same dc-link battery V_{dc}. In fig 1 each switch S_{A1} to S_{A8} and S'_{A1} to S'_{A8} consist of a power semiconductor device (e.g. MOSFET, GTO and IGBT etc) with connected in anti-parallel diode. Voltages Vc1, Vc2, Vc3, Vc4, Vc5, Vc6, and Vc7, are

$\frac{7}{8}V_{dc}, \frac{3}{4}V_{dc}, \frac{5}{8}V_{dc}, \frac{V_{dc}}{2}, \frac{3}{8}V_{dc}, \frac{V_{dc}}{4}$, and $\frac{V_{dc}}{8}$

respectively, as $n = 9$.

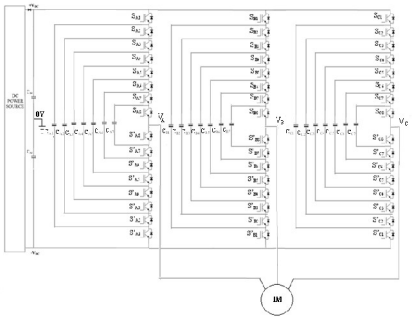

Figure 2. Nine-level FCMLI fed three phases Induction motor.

The main dc capacitor combination C is the energy storage element, while capacitors C_{A1}, C_{A2}, C_{A3}, C_{A4}, C_{A5}, CA6 and C_{A7} are the flying capacitors that provide the multilevel voltage ability to the converter. S_{kj} and S'_{kj} are the complementary switches where j=1 to 8 and k are A, B, C of phases respectively.Thus if S_{A1} is ON, S'_{A8} is OFF and vice-versa. For any initial state of clamping voltage, the inverter output voltage is given by

$$V_{an}=S_{A1}(V_{dc}-V_{C1})+S_{A2}(V_{C1}-V_{C2})+S_{A3}(V_{C2}-V_{C3})+S_{A4}(V_{C3}-V_{C4})+S_{A5}(V_{C4}-V_{C5})+S_{A6}(V_{C5}-V_{C6})+S_{A7}\left(V_{C6}-V_{C7}\right)+S_{A8}V_{C8}-\frac{V_{dc}}{2} \quad (3)$$

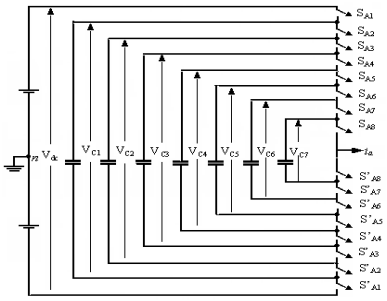

Figure 3. Phase-A leg of nine -level FCMLI.

B.Modulation Scheme

In this paper, control technique of sinusoidal pulse width modulation (SPWM) strategy is employed. In this method, a number of triangular waveforms are compared with a controlled sinusoidal modulating signal. The switching rules for the switches are decided by the intersection of the carrier waves with the modulating signal [8, 9, and 10]. The proposed nine level inverter, one modulating signal and eight carrier waves are necessary for each phase of the inverter as shown in Figure 4.

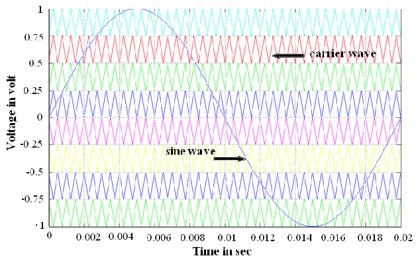

Figure 4. Modulation scheme for nine -levels

The modulating signal of each phase is displaced from each other by 120°. All the carrier signals have same frequency *fc* and amplitude *Ac* while the modulating signal has a frequency of *fm* and amplitude of *Am*.The *fc* should be in integer the multiples of *fm* with three-times. This is required for all the modulating signal of all the three phases see the same carriers, as they are 120° apart.

The carrier waves and the modulating signals are compared and the output of the comparator defines the output voltage waveform. It is assumed that the modulating signal varies from + 1V to – V.The amplitudes of the eight carriers waves vary in the step of ± 0.25V. In the positive half cycle the comparator output will have the value high, if the amplitude of the modulating signal is greater than that of the carrier wave and 0 otherwise. Similarly, for the negative half

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cycle if the modulating signal is lower than the carrier wave, the output of the comparator is high and 0 otherwise.

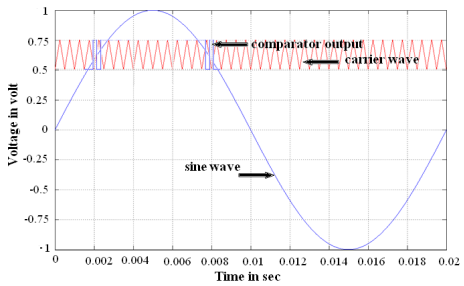

Figure 5. Switching voltage Technique for FCMLI

In the nine-level FCMLI each carrier waveform and sine waveform are compared individually. The Switching voltage Technique for FCMLI is shown in fig 5. The individual comparator output is given to the switching devices .An example of switching pulse generation simulation model is shown fig 6.As in fig 6 the comparator output is directly given to S_{A1} and S_{A1}' is connected through not gate, because S_{A1}' complementary operation of S_{A1}.

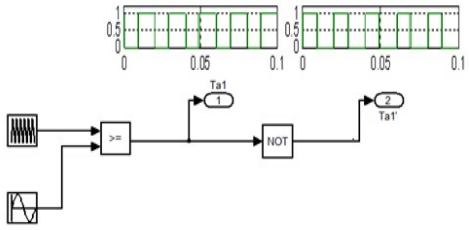

Figure 6. Simulation model for one switching pulse

In the nine-level FCMLI eight carrier waveform and a sine waveform are compared with comparator .This comparator output is given to S_{Aj} and S'_{Aj} switches where j=1 to 8. S'_{Aj} is the complementary function of S_{Aj}. In this way nine output levels are obtained. A Simulation model for switching pulses shown in Fig.6.It consists of eight carrier wave generators, a sine wave generator and relational operator. The outputs of each comparator for each phase are combined to produce the corresponding decision signals for the switches to synthesize the output voltage of that phase. The SPWM output reference signal is shown in Figure 5. This signal resembles with the output voltage waveform of the inverter and decides the voltage level, which is to be generated at a particular instant.

The nine-level FCMLI control circuit produce switching pulses for S_{Aj} and S'_{Aj} switches where j=1 to 8. S'_{Aj} is the complementary function of S_{Aj}. The sequence of the switching pulse turn-on the switching devices, and the FCMLI produce nine-level output voltage. The switching pulses for S_{Aj} and S'_{Aj} switches are shown in fig 7 and 8.

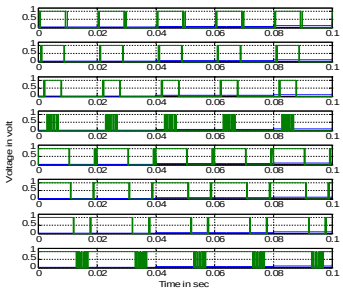

Figure 7. Switching pulses for S_{A1} to S_{A8}

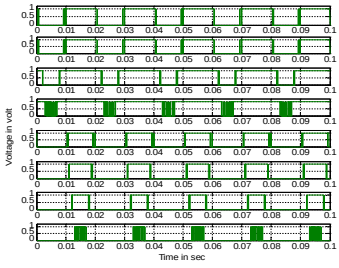

Figure 8. Switching pulses for S'_{A1} to S'_{A8}

III. PROPOSED SCHEME

In the paper, nine levels inverter is designed. The output voltages nearly get sinusoidal. It reduced harmonics and increase inverter efficiency. The implementation of ZVS or ZCS further reduces the switching loss. The nine level flying capacitor inverter fed induction motor drive has been developed by using MATLAB software.

IV. RESULT ANALYSIS

The nine-level FCMLI has been simulated using MATLAB. The output of the inverter voltage is shown in simulation results. Fig 10 shows the FCMLI phase voltage waveform. The stator of three phase induction motor is star connected.

A. Nine -Level FCMLI

The FCMLI output balanced phase voltage is 200Volts with nine levels as shown in figure 9.The line voltage is shown in fig10. It agrees with the conventional star connected stator voltage. Fig 11 exhibits the three phase stator voltage waveform. The nine step arrangement brought the simulation waveform in closed resemblance with the three phase sinusoidal waveform for the inverter parameters given in table I.

TABLE I
NINE -LEVEL INVERTER PARAMETERS

Number of main switches	48
Main devices type	IGBT
Device ON resistance	0.01 ohm
Device OFF resistance	1.0E6 ohm
Forward voltage drop	0 V
FCMLI capacitances	3600 µF

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The nine levels FCMLI phase have nine levels

$$(\frac{V_{dc}}{2}, \frac{3}{8}V_{dc}, \frac{V_{dc}}{4}, \frac{V_{dc}}{8}, 0, -\frac{V_{dc}}{2}, -\frac{3}{8}V_{dc}, -\frac{V_{dc}}{4}, -\frac{V_{dc}}{8})$$

and line to line voltages have fourteen levels.

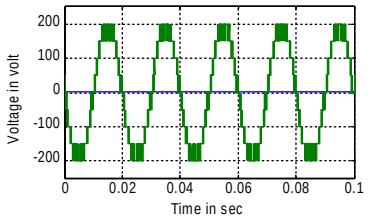

Figure 9. Phase voltage of FCMLI

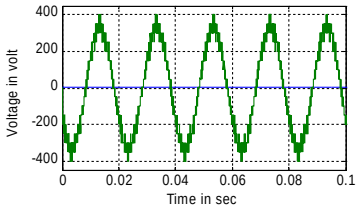

Figure 10. Line voltage of

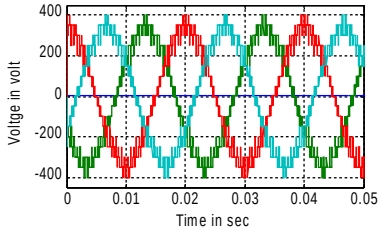

Figure 11. Three phase output line voltage of FCMLI

The fluctuation in capacitor voltage is tiny. This can be further reduced by increasing capacitance values and carrier frequency. Flying capacitor voltage Table II highlights the voltages across the capacitors.

TABLE. II
FLYING CAPACITORS VOLTAGE

Capacitors	Capacitors voltages
C_1	50 Volts
C_2	100 Volts
C_3	150 Volts
C_4	200 Volts
C_5	250 Volts
C_6	300 Volts

B. FCMLI fed Induction Motor

Induction motors are widely used in industries because it offers lot of advantages. The proposed method of a nine -level FCMLI is fed to induction motor drive of rating 5HP, 400V and supply frequency of 50Hz, speed of 1500rpm. A nine level FCMLI fed induction motor speed curve result shown in fig 12. It quickly settles to a constant speed. The stator current and electromagnetic torque are initially has maximum starting current then get reduced at rated value of the motor current.

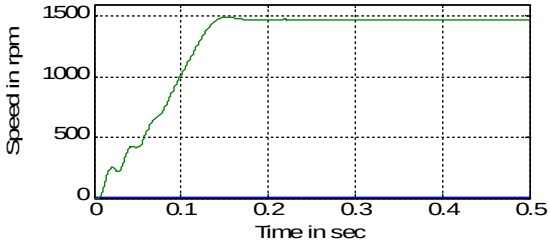

Figure 12 .Speed curve of induction motor

Total Harmonic Distortion of nine-level FLCMLI is 13.22% which is illustrated in figure 13. In the nine-level FCMLI, THD is reduced compared to THD value of five and seven -level FCMLI. The THD value of five and seven are 26.26% and 17.76% respectively. Different level of FCMLI THD values are compared it shown in table III. It have obtained same simulation parameters values

TABLE III COM PARISON OF THD

Five-level FCMLI (% of THD)	Seven-Level FCMLI (% of THD)	Nine-level FCMLI (% of THD)
26.26	17.76	13.22

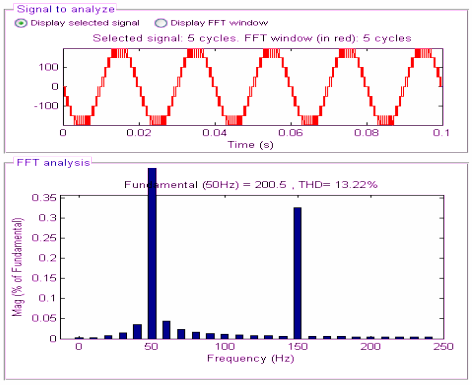

Figure.13 THD of nine levels FCMLI.

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V.CONCLUSION

In the proposed method, nine levels flying capacitor multilevel inverter provides sinusoidal waveform and increased efficiency. The basic concepts and operational features of inverter have been explored. A control scheme has been proposed which uses the preferential charging or discharging of flying the capacitors to balance their voltages. The control scheme allows balanced flying capacitor voltages; hence output phase and line voltages are obtained with much less THD. The nine level flying capacitor multilevel inverter fed induction motor has been illustrated with
simulation results using MATLAB. The technique is used to improve the level of the inverter to extend the design flexibility and reduces the harmonics.

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VI. BIOGRAPHIES

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